AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A method for manufacturing a semiconductor device, comprising:

forming first and second insulating gate portions to be spaced from each other on a semiconductor substrate, the first insulating gate portion including a first gate insulating film and a first gate electrode doped with an impurity of a first conductivity type, and the second insulating gate portion including a second gate insulating film and a second gate electrode doped with an impurity of a second conductivity type;

selectively implanting impurity ions of the first conductivity type to the first gate electrode and a surface layer of the semiconductor substrate adjacent to the first insulating gate portion;

selectively implanting impurity ions of the second conductivity type to the second gate electrode and the surface layer adjacent to the second insulating gate portion;

after implanting the impurity ions of the first and second conductivity types, performing pre-annealing at a first substrate temperature; and

after the pre-annealing, performing main activation for the impurity ions of the first and second types at a second substrate temperature higher than the first substrate temperature for a treatment period shorter than a period of the pre-annealing.

2. (Original) The method of claim 1, wherein the forming first and second insulating gate portions comprises:

forming an insulating film on the semiconductor substrate;

forming a polycrystalline conductive film doped with the impurity of the first conductivity type on the insulating film; and

selectively removing the insulating film and the polycrystalline conductive film to form the first and second gate insulating films and the first and second gate electrodes.

3. (Original) The method of claim 2, wherein the forming first and second insulating gate portions further comprises forming first and second sidewall spacers on the semiconductor substrate, the first sidewall spacer being adjacent to the first gate insulating film and the first gate electrode, and the second sidewall spacer being adjacent to the second gate insulating film and the second gate electrode.

4. (Original) The method of claim 2, wherein the forming a polycrystalline conductive film comprises:

depositing a polycrystalline conductive film made substantially of an intrinsic semiconductor on the insulating film;

implanting the impurity ions of the first conductivity type at least to a region where the first gate electrode is formed in the polycrystalline conductive film; and

diffusing the impurity ions of the first conductivity type into the polycrystalline conductive film.

5. (Original) The method of claim 3, wherein the selectively implanting impurity ions of the first conductivity type comprises:

selectively implanting the impurity ions of the first conductivity type to the first gate electrode and the surface layer adjacent to the first gate electrode; and

selectively implanting the impurity ions of the first conductivity type to the surface layer and the first gate electrode, both of which are adjacent to the first sidewall spacer.

6. (Currently amended) The method of claim 5 ~~further comprising~~, wherein selectively implanting impurity ions of the first conductivity type further comprises performing sub-activation for the impurity ions of the first conductivity type at the second substrate temperature for a treatment period shorter than the period of the pre-annealing after selectively implanting the impurity ions of the first conductivity type to the first gate electrode and the surface layer adjacent to the first gate electrode, and before selectively implanting the impurity ions of the first conductivity type to the surface layer and the first gate electrode~~, both of which are adjacent to the first sidewall spacer~~.

7. (Original) The method of claim 3, wherein the selectively implanting impurity ions of the second conductivity type comprises:

selectively implanting the impurity ions of the second conductivity type to the second gate electrode and the surface layer adjacent to the second gate electrode; and

selectively implanting the impurity ions of the second conductivity type to the surface layer and the second gate electrode, both of which are adjacent to the second sidewall spacer.

8. (Currently amended) The method of claim 7 ~~further comprising~~, wherein selectively implanting impurity ions of the second conductivity type further comprises performing sub-activation for the impurity ions of the second conductivity type at the second substrate temperature for the treatment period shorter than the period of the pre-annealing after selectively implanting the impurity ions of the second conductivity type to the second gate electrode and the surface layer adjacent to the second gate electrode, and before selectively implanting the impurity ions of the second conductivity type to the surface layer and the second gate electrode~~, both of which are adjacent to the second sidewall spacer~~.

9. (Currently amended) The method of claim 1, wherein the first substrate temperature T_1 (°C) and the treatment period t_{pa} (sec) of the pre-annealing satisfy a relationship represented by a following equation:

$$5\times10^{-8}\exp[2.21\times10^{4}/(T_1+275)]\leq t_{pa}$$
$$\leq 6\times10^{-13}\exp[3.74\times10^{4}/(T_1+275)].$$

10. (Original) The method of claim 9, wherein the first substrate temperature ranges from 600°C to 900°C.

11. (Original) The method of claim 9, wherein the treatment period of the pre-annealing ranges from 5 seconds to 3.6×10^{3} seconds.

12. (Original) The method of claim 4, wherein the pre-annealing and the diffusing the impurity ions of the first conductivity type into the polycrystalline conductive film are performed by use of any of an infrared lamp, and an electric furnace and hot plate operated by resistance heating.

13. (Original) The method of claim 1, wherein the treatment period of the main activation is 100 ms or less.

14. (Original) The method of claim 13, wherein surface density of irradiation energy of light emitted from a light source for use in the main activation on a surface of the semiconductor substrate is 100 J/cm^2 or less.

15. (Original) The method of claim 14, wherein the light source is a flash lamp into which a rare gas is enveloped.

16. (Original) The method of claim 14, wherein the light source is an excimer laser or a YAG laser, each oscillating a laser beam in a pulse shape.

17. (Original) The method of claim 4 further comprising performing pre-heating at a third substrate temperature approximately equal to/less than a temperature at the diffusing the impurity ions of the first conductivity type into the polycrystalline conductive film before the main activation, wherein the main activation is performed subsequently to the pre-heating.

18. (Original) The method of claim 17, wherein the third substrate temperature ranges from 200°C to 600°C.

19. (Original) The method of claim 17, wherein the pre-heating is performed by an infrared lamp or a hot plate.